ISO9002 Certified SCI Quality System

Sierra Components, Inc.

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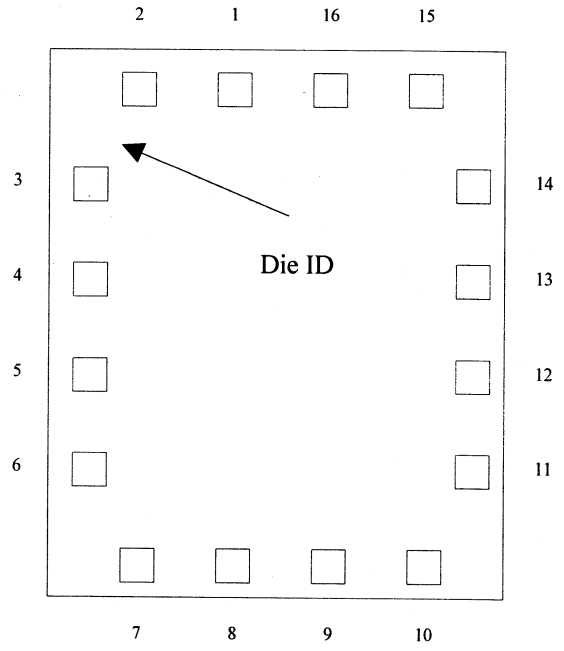
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



72 mils

51 mils

PAD	FUNCTION
1	N. CLR
2	1Q
3	N. 1Q
4	1D
5	2D
6	N. 2Q
7	2Q
8	GND
9	CLK
10	3Q
11	N. 3Q
12	3D
13	4D
14	N. 4Q
15	4Q
16	V_{CC}

Topside Metal: Al
Backside: Si
Backside Potential: Isolated
Mask Ref:
Bond Pads (Mils): 4 x 4

APPROVED BY:	**DIE SIZE (Mils): 51 x 72**	**DATE: 6/8/01**
MFG: Texas Inst	**THICKNESS: 12**	**P/N: 74HC175**